Reg. No. : | | | | | | | | | | | |

Question Paper Code : 66285

B.E./B.Tech DEGREE EXAMINATION, NOVEMBER/DECEMBER 2011.

Fourth Semester

Computer Science and Engineering

CS 2253 — COMPUTER ORGANIZATION AND ARCHITECTURE

(Common to Information Technology)

(Regulation 2008)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. Define word length.
2. What are the merits and demerits of single address instructions?
3. List the advantages of multibus organization.
4. What are the inputs for hardwired control?
5. What is the role of cache in pipelining?
6. What would be the effect, if we increase the number of pipelining stages?
7. What is DDR SDRAM?
8. What is TLB?
9. What are the components of an I/O interface?
10. Define SCSI.

PART B — (5 × 16 = 80 marks)

11. (a) (i) Discuss the factors influencing performance. (8)

(ii) Define addressing mode and explain the basic addressing modes with an example for each. (8)

Or

(b) State and explain the rules in arithmetic operations on floating point numbers.

12. (a) List and explain the steps involved in the execution of a complete instruction.

Or

(b) Draw necessary diagrams and explain the control signal generation using micro programmed control.

13. (a) What is a data hazard? How do you overcome it? And discuss its side effects.

Or

(b) Discuss the data and control path methods in pipelining.

14. (a) Explain different types of mapping functions in cache memory.

Or

(b) Discuss the following

(i) Interleaving (5)

(ii) Hit rate and Miss penalty (6)

(iii) Pre-fetching (5)

15. (a) (i) What are the steps in handling interrupts? (6)

(ii) With a neat sketch explain the working principle of DMA. (10)

Or

(b) Explain the working of PCI interface.

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